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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,419	DIFFENDERFER, JAN C.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-16 and 18-24 is/are rejected.

7)☒ Claim(s) 3 and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4 and 18 are objected to because of the following informalities:

In line 2, ""0 volts" should be replaced with – 0 volt –.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 5-6 and 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 is indefinite because it is not clear how a range of the higher voltage external output can exceed a range of the low voltage core input signals **by a factor of approximately three.**

Claims 6 and 19-20 are similarly rejected as claim 5.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, 9-10, 16, 19, 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Forbes (U.S Patent No. 6,288,575).

Forbes discloses in fig. 6A a pseudo-differential current sense amplifier including:

Regarding claim 1:

a low voltage input stage (M5, M6, I1, I2) that receives low voltage core input signals;

an output stage (M3, M4) that provides a higher voltage external output based on the low voltage core input signals; and

a cascade stage (M1, M2) coupled between the low voltage input stage (M5, M6) and the output stage (M3, M4) that provides a bias (inherent seen in 7) to the output stage (2) and provides a limit for preventing breakdown in the low voltage input stage.

Regarding claim 2: a feedback device (M7) coupled to the output stage (M3, M4) that prevents static current after a change in value of the external output.

Regarding claim 5: Fig. 6A in Forbes is capable to provide "a range of the higher voltage external output can exceed a range of the low voltage core input signals". Due to indefiniteness, the limitation "by a factor of approximately three" recited therein can not given sufficient weight to read over the reference.

Regarding claim 9: the output stage is a current mirror (M3, M4) comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

Regarding claim 10: the cascade stage is comprised of a pair of transistors (M1, M2) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (M3, M4).

Claim 16 is similarly rejected as claims 1 and 2:

a low voltage input stage (M5, M6, I1, I2) that receives low voltage core input signals;

an output stage (M3, M4) that provides a higher voltage external output based on the low voltage core input signals; and

a cascade stage (M1, M2) coupled between the low voltage input stage (M5, M6) and the output stage (M3, M4) that provides a bias (7) to the output stage (2);

a feedback device (M7) coupled to the output stage (M3, M4).

Claim 19 is similarly rejected as claim 5.

Regarding claim 22: the bias (7) is capable provided to the output stage provides a limit for preventing breakdown in the low voltage input stage (M5, M6).

Regarding claim 23: the feedback device (M7) prevents static current after a change in value of the external output.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamaki (U.S 2004/0061525).

Tamaki discloses in fig. 2 a voltage level shifting circuit including:

a low voltage input stage (215, 217) that receives low voltage core input signals;

an output stage (211, 213) that provides a higher voltage external output based on the low voltage core input signals; and

a cascade stage (219, 221) coupled between the low voltage input stage (215, 217) and the output stage (211, 213) that provides a bias to the output stage (C) and provides a limit for preventing breakdown in the low voltage input stage.

Regarding claim 5: Fig. 2 in Tamaki is capable to provide "a range of the higher voltage external output can exceed a range of the low voltage core input signals". Due to indefiniteness, the limitation "by a factor of approximately three" recited therein can not given sufficient weight to read over the reference.

Regarding claim 8: the low voltage input stage (215, 217) is comprised of a pair of low-voltage transistors having gates respectively coupled to a pair of differential signals (In, 207, 209) corresponding to the low voltage core input signals.

Regarding claim 9: the output stage is a current mirror (211, 213) comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

Regarding claim 10: the cascade stage is comprised of a pair of transistors (219, 221) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (211, 213).

Regarding claim 11: the low voltage input stage (215, 217) is comprised of a first pair of low-voltage transistors having gates respectively coupled to a pair of differential signals (In, 207, 209) corresponding to the low voltage core input signals, and

wherein the output stage is a current mirror (211, 213) comprised of a second pair of transistors having threshold voltages in accordance with the higher voltage external output, and

wherein the cascade stage is comprised of a third pair of transistors (219, 221) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (211, 213).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6-7, 13-14, 18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes as applied to claims 1 and 16 above.

As noted above, every element of the claimed invention recited in above claims can be seen in the circuit of Forbes. However, these references do not specifically disclose "a range of the low voltage core input signals is limited to between approximately 0 volt and 1 volts" as recited in claims 4 and 18; "the range of the higher voltage external output is between approximately 0 volt and 3.3 volts" as recited in claims 7 and 21.

Regarding claim 4: Although Forbes does not expressly state the range of the low voltage core input signals is limited to between approximately 0 volt and 1 volts, this difference is not of patentable merit because it is notoriously well known in the art that different values/range for the low voltage core input signals can be selected/limited in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize low voltage core input signals is limited to between approximately 0 volt and 1 volts in

realizing the circuit of the Forbes reference for the purpose of producing different output values when limited range is selected.

Regarding claim 6: Fig. 6A in Forbes is capable to provide "a range of the higher voltage external output can exceed a range of the low voltage core input signals". Due to indefiniteness, the limitation "by a factor of approximately three" recited therein can not given sufficient weight to read over the reference.

The same motivation applied to claim 4 is applied to claim 7: it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the range of the higher voltage external output is between approximately 0 volt and 3.3 volts in realizing the circuit of the Forbes reference for the purpose of producing different output values when different value of the range is selected.

Regarding claim 13: the output stage is a current mirror (M3, M4) comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

Regarding claim 14: the cascade stage is comprised of a pair of transistors (M1, M2) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (M3, M4).

Claim 18 is similarly rejected as claim 4.

Claim 20 is similarly rejected as claim 6.

Claim 21 is similarly rejected as claim 7.

Claims 4, 6-7, 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki as applied to claim 1.

The same motivation applied to Forbes is applied to Tamaki regarding claim 4: Although Tamaki does not expressly state the range of the low voltage core input signals is limited to between approximately 0 volt and 1 volts, this difference is not of patentable merit because it is notoriously well known in the art that different values/range for the low voltage core input signals can be selected/limited in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize low voltage core input signals is limited to between approximately 0 volt and 1 volts in realizing the circuit of the Tamaki reference for the purpose of producing different output values when limited range is selected.

Regarding claim 6: Fig. 2 of Tamaki is capable to provide "a range of the higher voltage external output can exceed a range of the low voltage core input signals". Due to indefiniteness, the limitation "by a factor of approximately three" recited therein can not given sufficient weight to read over the reference.

The same motivation applied to claim 4 is applied to claim 7: it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the range of the higher voltage external output is between approximately 0 volt and 3.3 volts in realizing the circuit of the Tamaki reference for the purpose of producing different output values when different value of the range is selected.

Regarding claim 12: the low voltage input stage (215, 217) is comprised of a pair of low-voltage transistors having gates respectively coupled to a pair of differential signals (In, 207, 209) corresponding to the low voltage core input signals.

Regarding claim 13: the output stage is a current mirror (211, 213) comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

Regarding claim 14: the cascode stage is comprised of a pair of transistors (219, 221) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (211, 213).

Regarding claim 15: the low voltage input stage (215, 217) is comprised of a first pair of low-voltage transistors having gates respectively coupled to a pair of differential signals (In, 207, 209) corresponding to the low voltage core input signals, and

wherein the output stage is a current mirror (211, 213) comprised of a second pair of transistors having threshold voltages in accordance with the higher voltage external output, and

wherein the cascode stage is comprised of a third pair of transistors (219, 221) having threshold voltages approximately the same as the threshold voltages of the current mirror transistors (211, 213).

Allowable Subject Matter

Claims 3 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

April 12, 2005